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IFD

June 25, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants: Praveen K. Samudrala

Serial No.: 10/708,268

Filing Date: 02/20/2004

For: Method and Apparatus for Creating Circuit Redundancy in Programmable Logic Devices

Our Reference No.: 1372.136.PRC

Examiner: Unassigned

Art Unit: 2816

Dear Sir:

Enclosed please find the following:

1. Information Disclosure Statement By Applicants- 2 pages;
2. Copies of two (2) U.S. Patent Documents;
3. Copies of the front covers of nine (9) Non-Patent Literature Documents; and
4. Self-addressed, postage prepaid post card to serve as a receipt for items 1-3.

Very respectfully,

SMITH & HOPEN

By: Molly L. Sauter
molly.sauter@smithhopen.com

MLS/cm
enclosure

CERTIFICATE OF MAILING
(37 C.F.R. 1.8)

I HEREBY CERTIFY that this correspondence is being mailed with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 25, 2004.

Date: June 25, 2004

Charlene Morgan

Attorney-Client Privileged Communication



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Substitute for form 1449/PTO

(Use as many sheets as necessary)

Complete if Known

Application Number	10/708,268
Filing Date	02/20/2004
First Named Inventor	Praveen K. Samudrala
Art Unit	2816
Examiner Name	Unassigned
Attorney Docket Number	1372.136.PRC

Sheet 1 of 2

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

[illegible]

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

THIS collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/708,268
				Filing Date	02/20/2004
				First Named Inventor	Praveen K. Samudrala
				Art Unit	2816
				Examiner Name	Unassigned
Sheet	2	of	2	Attorney Docket Number	1372.136.PRC

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	EDUARDO AUGUSTO BEZERRA ET AL., Improving Reconfigurable Systems Reliability by Combining Periodical Test and Redundancy Techniques: A Case Study.	
	2	ZOLTAN MEGGYESI ET AL., FPGA Design in the Presence of Single Event Upsets, CERN, Geneva, Switerland.	
	3	Single Event Upset (SEU) Mitigation by Virtual Triple Modular Redundancy (TMR) in Design Reduces Manufacturing Cost and Lowers Power, Alternative System Concepts, Inc., pg 1-7	
	4	EARL FULLER ET AL., Radiation Testing Update, SEU Mitigation, and Availability Analysis of the Virtex FPGA for Space Reconfigurable Computing, pg. 1-11.	
	5	K. NIKOLIC ET AL., Fault-Tolerant Techniques for Nanocomputers, TNT2001, Sept. 3-7, 2001, Segovia, Spain.	
	6	CARL CARMICHEAL ET AL., SEU Mitigation Techniques for Virtex FPGAs in Space Application.	
	7	PRAVEEN SAMUDRALA ET AL., Single Event Upsets and Mitigation Technigues: A Survey, pages 1-15.	
	8	SRINIVAS KATKOORI, SEU Tolerant Design Techniques for Space Based RC Implementations, IR & D Project, March 28, 2001.	
	9	PRAVEEN K. SAMUDRALA, Synthesis of SEU Tolerant FPGAs, January 22, 2003, pages 1-53.	

Examiner Signature		Date Considered	
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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